Journal of Dynamical Systems and Complexity (2026) vol.1(3): 23-35
eISSN: 3122-4326, DOI: 10.66131/JDSC12202623-35

Experimental Evaluation of a Hartley Oscillator Incorporating a Commercial SDC Memristor

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Abstract

This paper experimentally investigates the integration of a commercial Self-Directed Channel (SDC) memristor into a Hartley oscillator. While most existing literature relies on theoretical models or emulators, this work utilizes a physical W-type (tungsten-based) memristor to analyze its direct impact on the oscillator's periodic steady-state response. The experimental setup, implemented with a TL081CD operational amplifier and an Analog Discovery Studio platform, demonstrates that the memristor acts as a dynamic feedback element. Comparative results show that including the memristive device increases the peak-to-peak amplitude by 34% (from 2.724 V to 3.65 V) and shifts the frequency down from 14.530 kHz to 14.213 kHz. Furthermore, the memristor-based oscillator showed an additional startup interval of about 2 s, with an estimated relative variation of ±27% across repeated experiments. This behavior suggests a modified oscillator transient response, potentially linked to the SDC device's history-dependent electrical characteristics. The results indicate that the memristor-augmented Hartley oscillator maintains a stable sinusoidal waveform, suggesting that the device's state-dependent resistance can effectively modulate the system's gain and resonance conditions in analog circuit architectures.

Keywords— memristor, Hartley oscillator, frequency, amplitude

1 Introduction

Electronic oscillators are fundamental building blocks in modern engineering, generating periodic signals without external excitation. These circuits are widely used in communication systems, instrumentation, and signal processing, and serve as timing references in electronics. Among these topologies, LC-resonant oscillators are particularly important for producing stable, high-frequency waveforms.

A prominent member of this family is the Hartley oscillator, which uses a resonant tank circuit with a capacitor in parallel with a tapped inductor to set its oscillation frequency. The inductive

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Received: Jun 24, 2026, **Published:** October 30, 2026
Editor: E. Campos-Cantón

element is typically implemented as two series-connected coils or a single coil with a tap, providing the feedback needed to sustain oscillations. This configuration satisfies the Barkhausen criterion: the total phase shift around the loop is zero, and the loop gain is greater than or equal to unity.

A key advantage of the Hartley topology is its simplicity: it requires fewer components than other LC oscillators while still providing stable sinusoidal outputs over a wide frequency range. Its inductive feedback also makes it suitable for high-frequency and radio-frequency signal-generation and communication applications.

The memristor has emerged as the fourth fundamental passive element, complementing the resistor, capacitor, and inductor [1]. Chua predicted that, apart from resistors, capacitors, and inductors, a fourth fundamental passive circuit element should exist: the memristor, defined by the constitutive relationship between electric charge and magnetic flux [2]. It has a nonlinear voltage-current relationship and state-dependent resistance (memristance), offering unique properties for neuromorphic computing, non-volatile memory, and adaptive electronic systems [3, 4].

In 2008, researchers at Hewlett-Packard Labs announced one of the first physical solid-state memristors. Since then, interest in exploiting this emerging circuit element has grown, especially in analog circuitry and non-volatile memory applications [2].

In 2015, the American company Knowm Inc. designed and produced the world's first Knowm memristor packaged as a chip. Unlike the oxygen-vacancy migration technology used in HP memristors, Knowm memristors use metal-ion migration for electrical switching [4]. Knowm memristors provide researchers with a commercially available, effective device for related application studies [5].

While recent studies have explored integrating memristors into oscillator circuits to modulate their dynamics, much of this research remains grounded in theoretical models or emulators [6, 7, 8, 9, 10]. Experimental implementations of physical, discrete memristive devices remain relatively scarce. Unlike idealized models, physical memristors exhibit non-ideal dynamics that depend on excitation frequency, polarity, and prior stimulus history, which may critically influence the operation of resonant oscillators [4, 11].

This work investigates a Hartley oscillator incorporating a commercial memristor (Knowm Inc.) in its feedback network. The study moves from circuit simulations to experimental validation, examining the memristor's impact on critical parameters, including oscillation frequency, amplitude stability, and waveform symmetry.

2 Hartley Oscillator

Figure 1 shows the Hartley oscillator. It is a widely used LC oscillator topology that generates periodic signals through a resonant network of inductors and capacitors, combined with an amplifying stage that provides the feedback needed to sustain oscillations. Ralph V. L. Hartley originally proposed the circuit in the early twentieth century, and it has since been widely used in radio-frequency systems for its relatively simple configuration and ease of frequency tuning.

The equivalent inductance of the inductive network and the resonant-tank capacitance determine the Hartley oscillator's oscillation frequency. Under ideal conditions, the oscillation frequency can be approximated by:

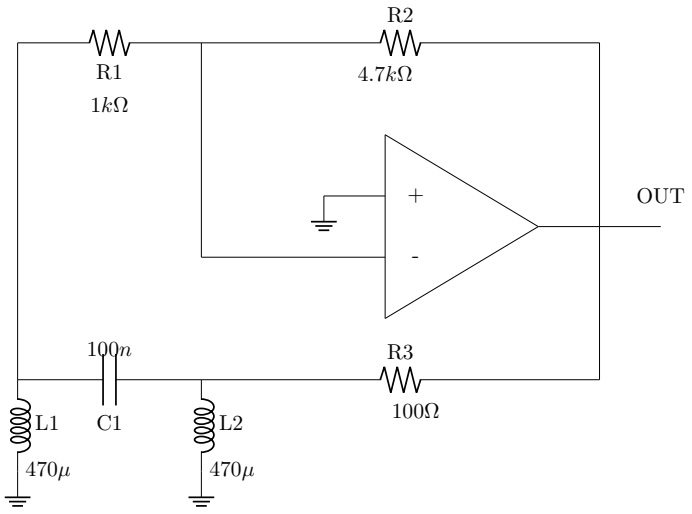


Figure 1: Hartley oscillator circuit.

$$f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}} \tag{1}$$

where L_1 and L_2 are the inductances of the series inductors, and C is the resonant capacitor's capacitance. By adjusting either the inductance or the capacitance, it is possible to tune the circuit's oscillation frequency.

One of the Hartley oscillator's main advantages is its simple design and frequency tunability. However, practical implementations may deviate from the ideal sinusoidal waveform due to component tolerances, nonlinearities in the active device, and parasitic effects in the circuit.

From a system-level perspective, incorporating a memristive device into the Hartley oscillator introduces a dynamic, state-dependent element into the feedback network. In the conventional topology, a fixed relationship between the inductive feedback ratio and the amplifier gain governs the oscillation condition, ensuring the Barkhausen criteria are satisfied under steady-state conditions. However, replacing or augmenting part of the feedback path with a memristor makes the effective resistance time-varying and history-dependent.

This modification directly affects the loop gain and the impedance seen by the resonant tank, allowing the memristor to modulate oscillation conditions in real time. As a result, key parameters such as amplitude stabilization, startup dynamics, and even the steady-state frequency may deviate from predictions of classical linear models. Unlike conventional resistive elements, the memristor exhibits nonlinear, adaptive behavior that can produce transient phenomena tied to internal-state evolution, such as delayed stabilization or gradual amplitude adjustment.

Therefore, integrating a physical memristor into the Hartley oscillator not only alters its electrical characteristics but also provides a platform for experimentally observing how state-dependent devices influence resonant systems beyond idealized assumptions.

3 Knowm W-type Memristor

The memristive device integrated into the Hartley oscillator is a commercial Self-Directed Channel (SDC) memristor from Knowm, Inc. The implementation uses a W-type (tungsten-based) memristor, whose hysteretic behavior is experimentally characterized using the Analog Discovery 2 Kit, as shown in Fig. 2. This hysteresis loop, observed in the current–voltage (I–V) relationship, is a defining feature of memristive systems and reflects the device's state-dependent resistance.

Unlike transition-metal oxide memristors that rely primarily on oxygen vacancy migration, the SDC memristor operates through the controlled movement of metal ions, typically silver (Ag^+), within a chalcogenide layer. This process forms and dissolves conductive filaments, dynamically modulating device resistance. As a result, the memristor exhibits a nonlinear, history-dependent response, making it particularly suitable for applications involving adaptive or time-varying behavior.

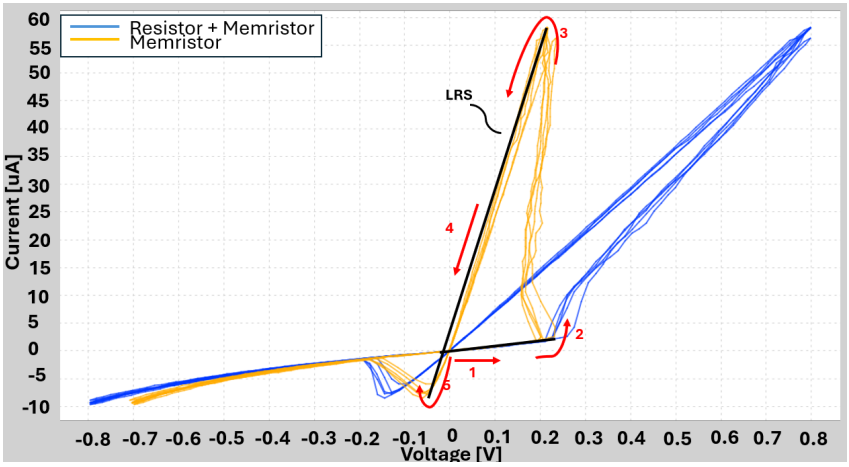


Figure 2: I–V characteristic of the Knowm memristor.

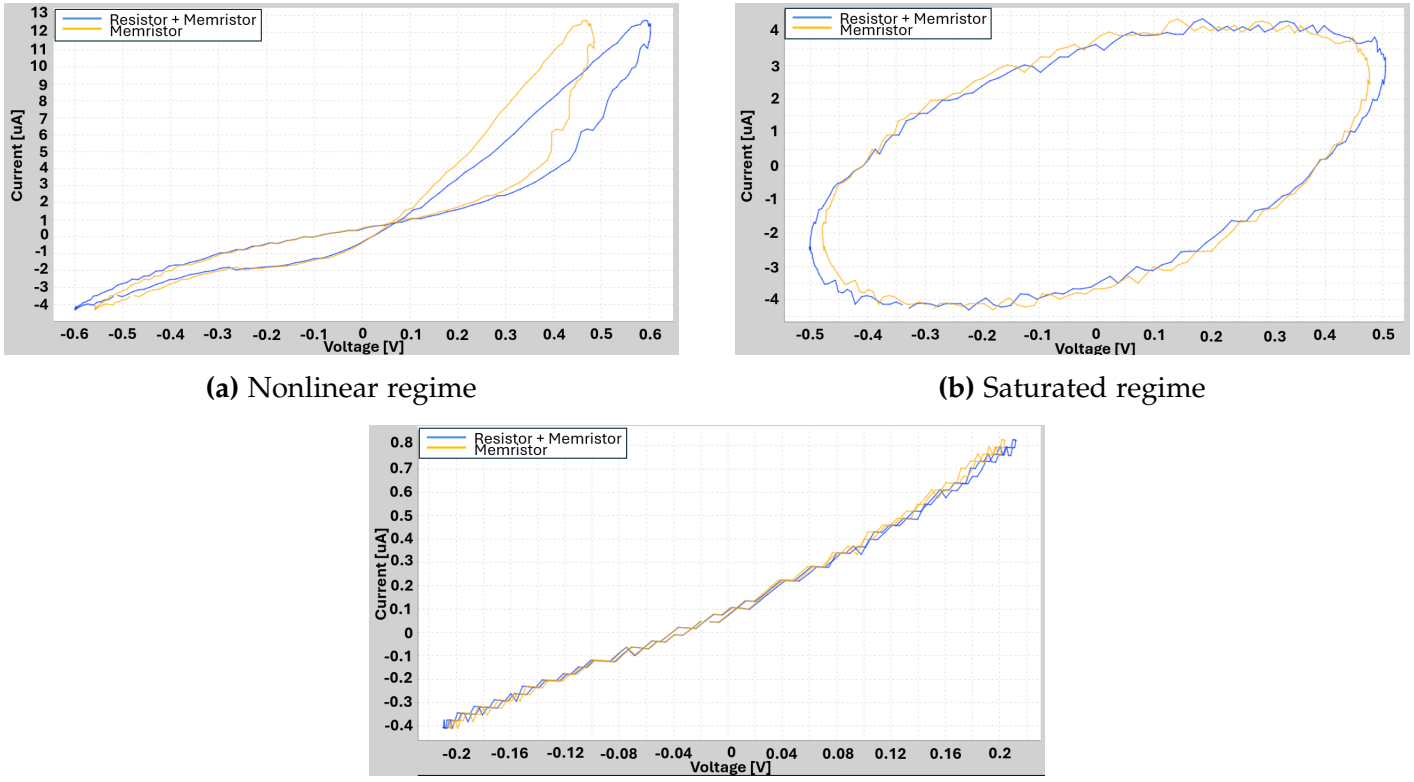
For this study, we estimated the memristor's effective resistance from the quasi-linear region of the measured I–V characteristic curve (Fig. 2) using Ohm's law, $R = V/I$. This characterization establishes an initial low-resistance state (Rinitial) of approximately $4\,\mathrm{k}\Omega$. This approximation provides a practical representation of the device within the operating region of interest, enabling its integration into the oscillator circuit analysis while preserving its dominant electrical behavior.

To ensure experimental consistency and mitigate the stochastic nature of filament formation, we applied a controlled state-reset protocol before measurements. The device recovers using a 10 Hz sinusoidal signal with an amplitude of 1 V. Additionally, a $-2\,\mathrm{V}$ is applied for 2 s, driving Ag^+ ions toward the anode and dissolving previously formed conductive filaments to restore the device to a reproducible baseline state.

This initialization process is critical to the Hartley oscillator's reliability, as it ensures the memristor starts from a well-defined resistance state before the dynamic feedback loop begins to influence its conductance. Because the oscillator's behavior is highly sensitive to variations in loop gain and impedance, uncertainty in the initial memristive state could significantly degrade frequency stability and amplitude response. This controlled initialization enables a more accurate evaluation of the memristor's impact on the oscillation dynamics.

To further assess the operational stability of the memristor-based oscillator, we evaluated continuous operation for up to 2 h. During these intervals, the oscillator maintained sustained oscillations without noticeable deviations in output behavior or operational failures and required no additional memristor resetting or retuning. We performed the reset and characterization procedures between experimental trials to establish comparable initial conditions, rather than in response to a loss of stability during operation. These observations suggest that, under the tested conditions, the commercial SDC memristor can remain functional within the oscillator for extended operating intervals without frequent readjustment. Nevertheless, the experiments do not establish their long-term stability beyond the evaluated duration.

3.1 Memristor Operating Window



(a) Nonlinear regime

(b) Saturated regime

(c) Quasi-linear regime

Figure 3: Initial experimental I–V characterization of the commercial Knowm W-type SDC memristor under sinusoidal excitation at different frequencies: (a) 10 kHz, exhibiting a nonlinear operating region; (b) 1 MHz, showing a saturated O-shaped response; and (c) 10 Hz, presenting a quasi-linear regime in which the device behaves predominantly as a resistance.

Before using it as a circuit element, we evaluated the Knowm W-type memristor under various excitation conditions to identify its practical operating window. This step is important because the device response depends not only on its intrinsic memristive properties but also on the applied voltage amplitude, excitation frequency, offset voltage, and initial resistive state. Therefore, a

memristor inserted into an oscillator should not be assumed to operate in a useful nonlinear regime without prior characterization.

Figure 3 shows representative I-V responses obtained during the initial characterization. Under suitable excitation conditions, the device exhibits a nonlinear hysteretic response, indicating active, observable memristive dynamics. However, outside this operating region, two limiting cases may appear. At low excitation levels, the hysteresis loop can collapse to a quasi-linear characteristic, causing the device to behave primarily as an equivalent resistor. In contrast, under other excitation conditions, the response can evolve into a closed O-shaped curve, associated with a saturated or strongly limited regime. In both cases, the dynamic memristive contribution becomes less distinguishable, which can lead to incorrect interpretations when the device is later integrated into an oscillator.

For this reason, we used the initial I-V characterization to select operating conditions where the memristor maintained a measurable nonlinear response before replacing individual resistors in the oscillator.

3.2 Mathematical Description of the Memristive Device

The Mean Metastable Switch (M-MSS) model developed by Knowm [12, 13] describes memristive behavior by representing resistance modulation through voltage-dependent transitions between metastable states. The model introduces an internal state variable x, ranging from 0 to 1, whose temporal evolution is expressed as

$$\frac{dx}{dt} = (1-x)P_{\mathrm{OFF}\to\mathrm{ON}} - xP_{\mathrm{ON}\to\mathrm{OFF}}, \tag{2}$$

where the transition rates are defined as

$$P_{\mathrm{OFF}\to\mathrm{ON}} = \frac{1}{\tau}\frac{1}{1+\exp\left[-\frac{V-V_{\mathrm{ON}}}{V_T}\right]}, \tag{3}$$

$$P_{\mathrm{ON}\to\mathrm{OFF}} = \frac{1}{\tau}\frac{1}{1+\exp\left[\frac{V+V_{\mathrm{OFF}}}{V_T}\right]}. \tag{4}$$

Here, V is the applied voltage, τ is the characteristic time constant, V_{ON} and V_{OFF} are switching parameters, and V_T is the thermal voltage.

The state-dependent conductance is given by

$$G(x) = \frac{x}{R_{\mathrm{ON}}} + \frac{1-x}{R_{\mathrm{OFF}}}, \tag{5}$$

where R_{ON} and R_{OFF} represent the limiting resistance states. Accordingly, the memristive current can be expressed as

$$I_M(V,x) = VG(x). \tag{6}$$

The M-MSS formulation also permits an additional nonlinear Schottky contribution to the total current. In this work, we introduce these relationships as a phenomenological description of

memristive behavior rather than a quantitatively calibrated representation of the specific Knowm W-type SDC device. We obtain the results presented here through direct experimental measurements on the physical memristor, without relying on numerical predictions from the mathematical model.

4 Experimental Implementation

This study used a discrete Knowm M+SDC device (W-type, tungsten-based) packaged in a 16-DIP configuration as the memristive element. Before integrating it into the oscillator, we characterized the device to verify its I–V hysteresis behavior and establish a reproducible initial low-resistance state (LRS), as described in the previous section. This preconditioning step is essential because filament formation in SDC memristors is stochastic.

For the memristor-augmented configuration, we inserted the device into the feedback path with a defined polarity, as shown in Fig. 4. This placement ensures that the oscillating voltage directly influences the internal ionic dynamics, allowing the memristance to evolve in response to circuit operation. Consequently, the memristor acts as a dynamic element within the feedback loop, modifying the effective gain and impedance during oscillation.

The Digilent Analog Discovery Studio powered and monitored the circuit, providing a stable, symmetrical $\pm 12\,\mathrm{V}$ supply to the active elements. The platform's integrated digital oscilloscope and waveform generator enabled real-time data acquisition and signal analysis, allowing precise characterization of the output waveforms in both the standard and memristor-augmented configurations.

To reduce instrumental errors and improve measurement accuracy, the Analog Discovery 2 was calibrated using WaveForms software and an external digital multimeter. The calibration procedure covered the waveform generators, acquisition channels, and power supplies. The resulting calibration parameters were stored by the device and applied to correct generated and acquired signals. This procedure helps mitigate systematic measurement errors.

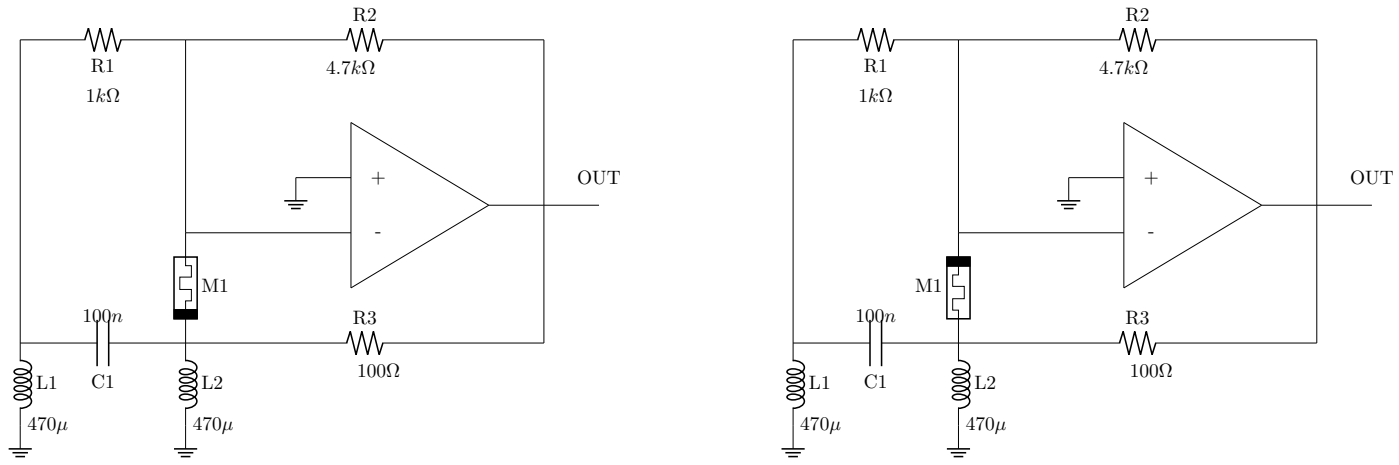
To ensure a fair comparison, we evaluated three configurations: the conventional Hartley oscillator and two memristor-based configurations that differed only in the polarity of the physical device. All other circuit components and connections remained unchanged, allowing us to examine how memristor orientation affects the oscillatory response experimentally.

For the Hartley oscillator, we evaluated two memristor-based configurations to analyze how device placement affects the output response. Figure 4 shows the corresponding circuits. In the first configuration, the oscillator maintained a frequency close to the standard circuit, changing from 14.530 kHz to 14.213 kHz.

In the second memristor-based configuration, the oscillator response changed more strongly. The output frequency increased to 18.11 kHz, while the maximum and minimum voltages reached 4.32 V and -4.315 V, respectively, resulting in a peak-to-peak voltage of 8.635 V.

Both circuits employ identical components and connection points, with the memristor occupying the same position within the oscillator. The only difference between the configurations is the device's orientation: in Case 1, the memristor is connected to its original polarity, whereas in Case 2, its polarity is reversed. This arrangement lets us evaluate the memristor orientation's influence on the oscillator response without changing the circuit topology or component values.

The oscillator's active core consists of a TL081CD operational amplifier. We selected this JFET-



(a) Memristor case 1 **(b)** Memristor case 2

Figure 4: Hartley oscillator circuits incorporating the memristor under two different configurations used in this work.

input device for its high input impedance and 13 V/μs slew rate, which prevent significant phase distortion or amplitude clipping at the target operating frequency of 14 kHz. As seen in Fig. 1, the resonant network was constructed using nominal values for all components, featuring two 470 μH inductors (L_1, L_2) and a 100 nF ceramic capacitor (C_1); the feedback and bias network was completed with a 1kΩ resistor (R_1), a 4.7kΩ resistor (R_2), and a 100Ω shunt resistor (R_3), the latter serving to stabilize the current path through the feedback loop. We conducted all measurements under steady environmental conditions and performed multiple trials to verify repeatability. We recorded and analyzed the output waveforms for frequency, amplitude, duty cycle, and transient response, enabling a comprehensive comparison between the conventional and memristive oscillator configurations.

5 Results and Discussion

The experimental evaluation of the Hartley oscillator revealed that integrating the W-type Knowm memristor produces configuration-dependent changes in the output response. As summarized in Table 1, we compared two memristor-based configurations with the standard LC oscillator to assess how device placement affects oscillation frequency, voltage swing, and temporal symmetry.

Repeatability was evaluated across eight experimental trials for each memristor configuration. The frequency coefficient of variation (CV) decreased from 1.67% in Case 1 to 1.26% in Case 2, indicating lower relative variability in frequency for the latter configuration. For the voltage measurements, the CVs of V_{max}, V_{min}, and V_{PP} were 6.52%, 8.27%, and 6.395% for Case 1, respectively, compared with 7.62%, 10.95%, and 9.257% for Case 2. These results indicate that, although Case 2 exhibited lower relative variability in frequency, its voltage-related measurements showed greater relative dispersion than those of Case 1. The results therefore reveal parameter-dependent repeatability across the two configurations.

In the first memristor configuration, the output amplitude changed most significantly. The

standard Hartley oscillator produced a peak-to-peak voltage of 2.724 V, whereas Memristor Case 1 increased this value to 3.65 V. This represents an approximately 34% increase in the voltage swing. Similarly, the amplitude increased from 1.36 V to 1.825 V. This behavior suggests that, in this configuration, the memristor modifies the oscillator's effective feedback conditions, increasing the output signal's steady-state energy level without forcing the waveform into supply-rail saturation.

Table 1: Performance comparison between the standard oscillator and two memristor-based oscillator cases.

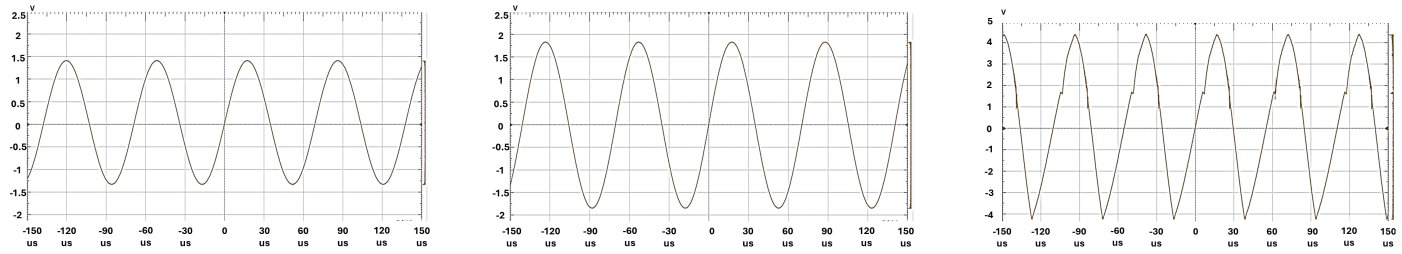
Parameter	Standard Oscillator	Memristor Case 1	Memristor Case 2
Frequency	14.530 kHz	14.213 kHz	18.11 kHz
Amplitude	1.36 V	1.825 V	4.318 V
V Max	1.415 V	1.8 V	4.32 V
V Min	-1.31 V	-1.85 V	-4.315 V
Vpp	2.724 V	3.65 V	8.635 V
PosDuty	50.04%	50.05%	51.33%
NegDuty	49.97%	49.95%	48.67%
PosWidth	34.435 μs	35.214 μs	29.015 μs
NegWidth	34.386 μs	35.146 μs	27.509 μs

Based on the nominal values of the resonant components ($L_1 = L_2 = 470$ μH and C1 = 100 nF), the conventional Hartley oscillator's theoretical oscillation frequency is approximately 16.42 kHz, assuming negligible mutual inductance between the inductors. The experimentally measured frequency was 14.530 kHz, representing a deviation of approximately -11.5% from the theoretical prediction. This discrepancy may result from non-ideal circuit characteristics, including component tolerances, parasitic impedances, and the operational amplifier's frequency-dependent response. These factors should be considered when comparing the ideal resonant frequency with the physical oscillator's measured behavior.

Memristor Case 1 showed a slight frequency reduction from 14.530 kHz to 14.213 kHz (2.18%), indicating that the Hartley oscillator's resonant behavior was largely preserved. This variation may reflect the SDC device's non-ideal electrical characteristics and its interaction with the feedback network. Waveform symmetry remained practically unchanged, with positive and negative duty cycles of 50.05% and 49.95%, respectively.

In contrast, Memristor Case 2 increased the oscillation frequency to 18.11 kHz (24.6% above the standard configuration) and the peak-to-peak voltage to 8.635 V, approximately 3.17 times the reference value. The corresponding amplitude reached 4.318 V. The waveform also showed moderate asymmetry, with positive and negative duty cycles of 51.33% and 48.67%, and pulse widths of 29.015 μs and 27.509 μs, respectively.

The two memristor-based configurations differ only in the device's polarity, while its position within the Hartley oscillator remains unchanged. Reversing the memristor polarity increased the frequency from 14.213 kHz to 18.110 kHz (approximately 27.4%) and the amplitude from 1.825 V to 4.318 V (approximately 136.6%). This polarity-dependent response is consistent with the asymmetric conductance-switching behavior of Knowm SDC memristors, where the applied voltage direction influences the evolution of the internal conductive state. Under alternating excitation,



(a) Standard Hartley oscillator waveform.

(b) Hartley oscillator including memristor (Case 1).

(c) Hartley oscillator including memristor (Case 2).

Figure 5: Experimental waveform comparison between the standard Hartley oscillator and two configurations incorporating the physical memristor, obtained using the Digilent Analog Discovery measurement system.

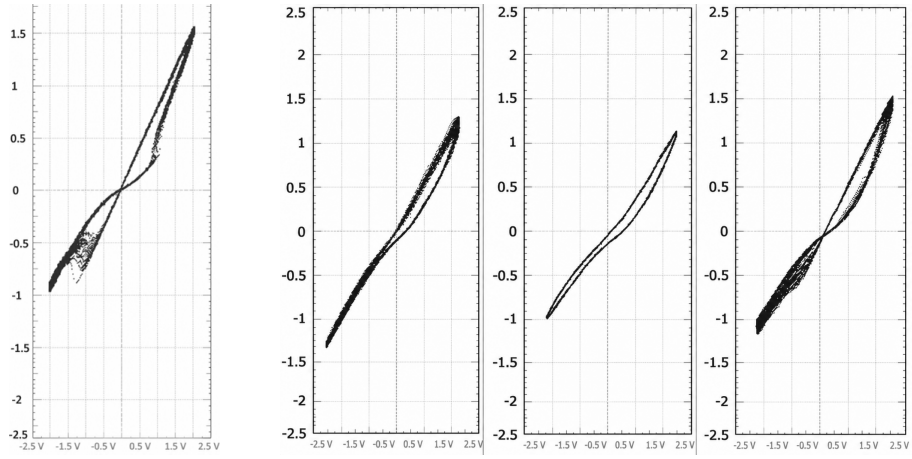
reversing the device orientation changes the relationship between the oscillator voltage and the memristor's conductance evolution, potentially modifying the circuit's effective impedance and feedback conditions.

These results show that the memristor does not behave as a simple passive replacement for a fixed resistor. Instead, its effect depends strongly on its position within the oscillator structure and on its interaction with the resonant and feedback paths. In Memristor Case 1, the device mainly increased the output amplitude while preserving the frequency and duty-cycle symmetry. In contrast, Memristor Case 2 produced a higher-frequency, higher-amplitude response but also introduced slight waveform asymmetry. Therefore, the Hartley oscillator confirms that integrating physical memristive devices can enable adaptive tuning. However, the resulting behavior must be interpreted in light of the specific circuit configuration and the memristor's operating region.

The memristor-based Hartley oscillator consistently showed an additional startup interval of approximately 2 s before reaching a stable oscillatory regime. We evaluated this behavior using two complementary methods: direct observation of the output waveform and subsequent analysis of the recorded numerical data. Across repeated experiments, the observed delay varied by approximately ±27% around the nominal 2 s value, corresponding to an estimated range of 1.46–2.54 s. Before each experiment, we reset and characterized the memristor to establish comparable initial operating conditions. This delay provides experimental evidence of the memristor's state evolution; the initial cycles of the oscillating voltage must provide sufficient charge flow to "train" or stabilize the silver filaments within the SDC layer. Once the memristance reaches its operational equilibrium, the waveform stabilizes into a remarkably pure sine wave, as shown in the oscilloscope captures given in Fig. 5. The absence of significant harmonic distortion, despite the increased amplitude, further confirms that the tungsten-based (W-type) memristor provides stable, reliable nonlinear regulation, making it a viable component for adaptive signal generation in LC topologies.

As an additional control, we replaced the physical memristor with a fixed resistor matching its initial resistance (4 kΩ), while keeping the remaining circuit components unchanged. Under these conditions, the Hartley oscillator operated at 15.737 kHz with a peak-to-peak voltage of 2.950 V. In comparison, the memristor-based configurations operated at 14.213 kHz and 18.110 kHz, with peak-to-peak voltages of 3.650 V and 8.635 V, respectively. These differences indicate that the initial resistance value alone is insufficient to reproduce the memristor-based oscillator's measured response.

During operation within the Hartley oscillator, the memristor exhibited a dynamic response near the boundary between the nonlinear and saturated regimes. The measured I–V trajectories showed variations between these two behaviors rather than remaining confined to a single stationary regime. This observation indicates that the operating conditions imposed by the oscillator do not necessarily correspond to a fixed memristive state.



(a) Case 1 **(b)** Case 2

Figure 6: I-V plot of the memristor during oscillator operation

6 Conclusions

We evaluated two memristor-based configurations that differ only in the device's polarity within the circuit. The results show that the memristor's physical orientation directly influences the oscillator dynamics, affecting not only the output amplitude but also the oscillation frequency and waveform symmetry.

In Memristor Case 1, the circuit preserved a frequency close to that of the standard Hartley oscillator. The frequency changed from 14.530 kHz to 14.213 kHz, a reduction of about 2.18%. However, the peak-to-peak voltage increased from 2.724 V to 3.65 V, representing an amplitude enhancement of approximately 34%. This indicates that, under this polarity, the memristor mainly modifies the effective feedback conditions and increases the steady-state voltage swing without significantly disturbing the waveform's temporal symmetry.

In contrast, Memristor Case 2 produced a stronger modification of the oscillator response. Reversing the memristor polarity increased the oscillation frequency to 18.11 kHz. It raised the peak-to-peak voltage to 8.635 V, corresponding to a frequency increase of approximately 24.6% and a voltage swing more than three times larger than that of the standard oscillator. In addition, the duty cycle changed from an almost symmetric condition to 51.33% positive duty and 48.67% negative duty, indicating that the reversed polarity introduces a moderate asymmetry in the oscillatory response.

A relevant observation was a startup transient before the system reached a stable oscillatory regime. This behavior suggests that the SDC memristor's internal state evolves during the first excitation cycles before reaching an operational equilibrium. Once it stabilizes, the oscillator can

maintain a stable sinusoidal output, showing that a physical memristive device can integrate into an LC oscillator while preserving sustained oscillation, provided it operates within an appropriate electrical regime.

Overall, these findings show that commercial memristors can serve as polarity- and state-dependent elements for tuning analog oscillator circuits. The comparison between the two memristor orientations confirms that the device does not behave as a simple fixed-resistance replacement; instead, its nonlinear, directional response interacts with the oscillator's feedback and resonant paths. Therefore, prior device characterization and careful consideration of memristor polarity are essential for correctly interpreting and designing memristor-based oscillator systems.

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